IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): An image processor comprising:

a control unit configured to control the transfer of image data to predetermined destinations;

a switch configured to divide the image data into m x n pixels based on a first command from the control unit, the image data having n lines with m pixels per ~~one~~ line, ~~and~~ the switch further configured to transfer each one of the n lines of the image data to [[a]] one of the predetermined ~~destination~~ destinations based on a second command from the control unit;

a storage unit including (n-1) number of memories each configured to store one line of the n lines of the image data;

~~a control unit configured to control the transfer of the each one of the n lines of the image data to the predetermined destination;~~

a compression unit configured to batch compress the image data of m x n pixels based on a third command from the control unit,

wherein said control unit is further configured to:

control said switch to directly transfer (n-1) lines of the n lines of the image data to a first destination of the predetermined destinations, the first destination being the (n-1) number of memories, ~~and~~

directly transfer a remaining one line of the n lines of the image data directly to a second destination of the predetermined destinations, the second destination being said compression unit; and

[[to]] control the storage unit to transfer the (n-1) lines of the image data stored in the (n-1) number of memories to said compression unit~~, and~~

~~wherein said transfer from the storage unit of the (n-1) lines of the image data stored in the (n-1) number of memories to said compression unit is performed~~ simultaneously with the direct transfer of said remaining one line of the n lines of the image data to said compression unit.

Claim 2 (Previously Presented): The image processor according to claim 1, wherein the (n-1) number of memories are (n-1) number of FIFO (first-in first-out) memories.

Claims 3-5 (Canceled).

Claim 6 (Currently Amended): An image processor comprising:

means for controlling the transfer of image data to a predetermined destination;

means for dividing image data into m x n pixels based on a command from the means for controlling, the image data having n lines with m pixels per one line;

means for transferring ~~without storing in the means for transferring~~ each one of n lines of the image data to [[a]] the predetermined destination based on a command from the means for controlling;

means for switching the predetermined destination for the each one of the n lines of the image data based on a command from the means for controlling;

means for storing (n-1) lines of the image data;

~~means for controlling the transfer of each one of the n lines of the image data to the predetermined destination;~~

means for batch compressing the image data of m x n pixels based on a command from the means for controlling,

wherein said means for controlling controls said means for switching to:

directly transfer (n-1) lines of the n lines of the image data to said means for storing, ~~and~~

directly transfer the remaining one line of the n lines of the image data directly to said means for batch compressing; and

~~controls~~ control the means for storing to transfer the (n-1) lines of the image data stored in the means for storing to said means for batch compressing~~, and~~

~~wherein said transfer from the means for storage of the (n-1) lines of the image data stored in the means for storing to said means for batch compressing is performed~~ simultaneously with the direct transfer of said remaining one line of the n lines of the image data to said means for batch processing.

Claim 7 (Previously Presented): The image processor according to claim 6, wherein said means for storing comprises (n-1) number of FIFO (first-in first-out) memories.

Claims 8-10 (Canceled).

Claim 11 (Currently Amended): An image processing method comprising:

controlling the transfer of image data to predetermined destinations;

dividing image data into m x n pixels based on a command from the controlling, the image data having n lines with m pixels per one line;

transferring each one of the n lines of the image data to [[a]] one of the predetermined ~~destination~~ destinations based on a command from the controlling;

switching the predetermined destination for the each one of the n lines of the image data based on a command from the controlling;

storing one line of the n lines of the image data in each of (n-1) number of memories;

batch compressing the image data of m x n pixels based on a command from the controlling,

wherein said transferring directly transfers (n-1) lines of the n lines of the image data to said (n-1) number of memories, [[and]]

said transferring directly transfers the remaining one line of the n lines of the image data directly to a compression unit based on said switching; and

said transferring transfers the (n-1) lines stored in the (n-1) number of memories to said compression unit~~, and~~

~~wherein said transferring of the (n-1) lines of the image data stored in the (n-1) number of memories to said compression unit is performed~~ simultaneously with the direct transfer of said remaining one line of the n lines of the image data to said compression unit.

Claims 12 and 13 (Canceled).